

IN THE CLAIMS:

Claim 1 (previously presented): a logic circuit, comprising:

a first inversion section for inverting a first input signal having one of positive logic and negative logic and outputting an inverted first input signal;
a second inversion section for inverting a second input signal having the other of the positive logic and the negative logic and outputting an inverted second input signal; and
a transmission section for selectively outputting one of the inverted first input signal of said first inversion section and the inverted second input signal of said second inversion section in accordance with a logical value which depends upon an externally controllable selection signal and an inverted signal of the selection signal.

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Claim 2 (original): A logic circuit, comprising:

a first inversion section for inverting a first input signal and outputting the inverted signal;
a second inversion section for inverting a second input signal and outputting the inverted signal;
a first outputting section for selectively outputting one of the output of said first inversion section and the output of said second inversion section in accordance with a logical value which depends upon an externally controllable first selection signal and an inverted signal of the first selection signal; and
a second outputting section for selectively outputting one of the output of said first inversion section and the output of said second inversion section in accordance with a logical value

which depends upon an externally controllable second selection signal and an inverted signal of the second selection signal.

Claims 3-6 (canceled)

Claim 7 (Currently amended): A logic circuit, comprising:

a first inversion section for inverting a first input signal and outputting the inverted signal;
a second inversion section for inverting the inverted signal of the first input signal and outputting a resulting signal;

a first outputting section for performing NANDing arithmetic between the output of said first inversion section and a second input signal and outputting a first resulting signal; and
a second outputting section for performing NANDing arithmetic between the output of said second inversion section and an inverted signal of the second input signal and outputting a second resulting signal;

said first outputting section and said second outputting section being switched with the second input signal and the inverted signal of the second input signal, said first outputting section outputs the second first resulting signal and said second outputting section outputs the first second resulting signal.

Claim 8 (original): The logic circuit as claimed in claim 1, further comprising:

a first switching section provided on an input side of said first inversion section and capable

of performing switching of whether the first input signal should be passed or blocked in accordance with an external control signal; and

a second switching section provided on an input side of said second inversion section and capable of performing switching of whether the second input signal should be passed or blocked in accordance with the external control signal.

Claims 9-12 (canceled)

Claim 13 (currently amended): A logic circuit, comprising:

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a first inversion section for inverting a first input signal having one of positive logic and negative logic and outputting an inverted first input signal, said first inversion section being essentially composed of transistor circuits, each of said transistor circuits having a first input signal terminal for the first input signal, a first input selection signal terminal for the ~~a~~ controllable selection signal and an outputting terminal for outputting the selection signal or the inverted signal based on the logic of the first input signal;

a second inversion section for inverting a second input signal, said second inversion section being essentially composed of transistor circuits, each of said transistor circuits having a second input signal terminal for the second input signal, a second input selection signal terminal for the controllable selection signal and an outputting terminal for outputting the selection signal or the inverted signal based on the logic of the first input signal;

a transmission section for selectively outputting one of the output of said first inversion

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section and the output of said second inversion section in accordance with a logical value which depends upon an externally controllable selection signal and an inverted signal of the selection signal.

Claim 14 (canceled)